BACKPLANE CONTROLLER WITH USB, SGPIO, DELL-PROTON, AND IPMI

GENERAL DESCRIPTIONo

The MG9088 is a low-cost, ultra-small, single-chip solution for use on SAS and SATA Backplanes for up to 8 drives per backplane. The chip features USB support and IPMI supports to the BMC through SMBUS. LED management utilizes the SGPIO protocol or DELL-PROTON.
Cascaded controllers can support up to 32 drives.

True Single Chip Solution – None of these components needed:

FEATURING

- Provides drive Activity, Fail/Rebuild and Locate LEDs for each drive
- Multiplexed SGPIO with the Drive Ready LED signal, to show Activity in non-RAID environments
- Built in Regulator for 5V operation. (Supply range 5.5V-2.7V)
- Small TQFP-48 Package (9mm X 9mm)
- IPMI/IPMB support to host BMC
- DELL-PROTON support
- Supports SGPIO Specification SFF-8485
- Supports Dell Proton blinking pattern
- Directly drives 2 LEDs for up to 8 slots
- Global Activity & Fail LED
- Internal Oscillator (no external crystal needed)
- Part ships ready to use, no firmware or programming required
- USB 2.0 compliant support for Status, Monitoring, Diagnostic, and FW update
- Firmware Upgradable or Configurable through USB or SMBus
- Diagnostics and FW tools available for Win32, Win64, Linux, EFI and DOS

SCOPE

This document is intended to assist designers and licensees of this product in the implementation and use of the product. It does not include information in how to develop software or detailed technical information or timing information.

CONTACT INFORMATION

See www.ami.com for contact information to your nearest representative.

PART ORDERING INFORMATION

Part Number	FW Version	Notes
MG9088-xxx	xxx	The xxx indicates the firmware version number of the part ordered. Contact AMI for available firmware releases.

See your nearest AMI representative for ordering information, pricing and support.

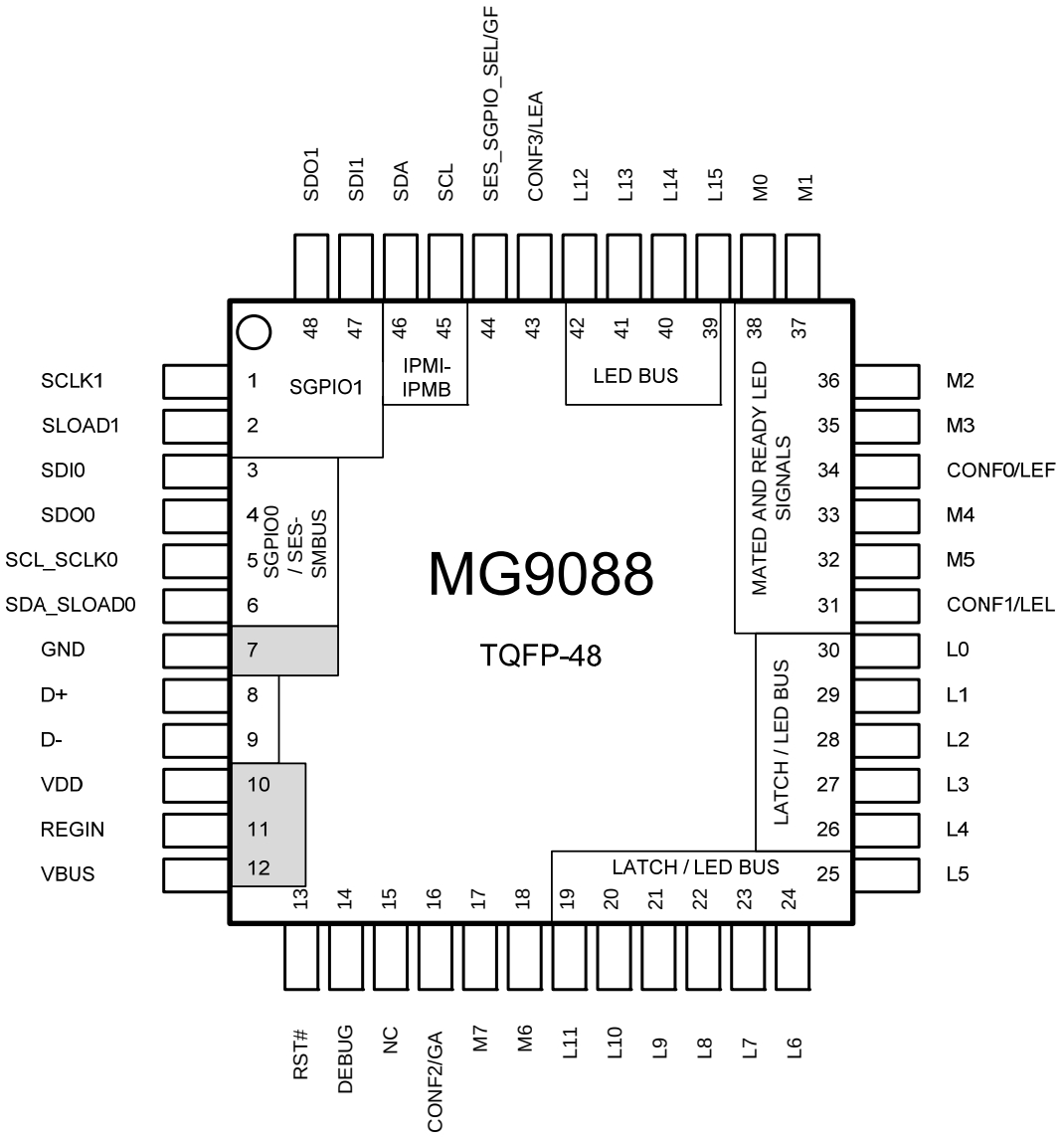
REVISION HISTORY

Date	Version	Created by	Description
08/02/11	0.1	Kayal D	Preliminary Draft
08/17/11	0.2	Kayal D & Shibu A	Updated section 1,2,5,6
08/23/11	0.3	Kayal D & Shibu A	Updated section 1,2,6
09/08/11	0.4	Kayal D	Updated section 1.1
09/22/11	0.5	Kayal D	Latch/No latch strapping added, conf 0x0A & 0x0B changed
10/05/11	0.6	Shibu A	Updated sections 2, 7 and 16.
04/19/12	0.7	Shibu A	Section 5 added, section 7 & 17 updated
05/22/12	0.8	Kayal D & Shibu A	Section 5, 8 and 17 updated

TABLE OF CONTENTS

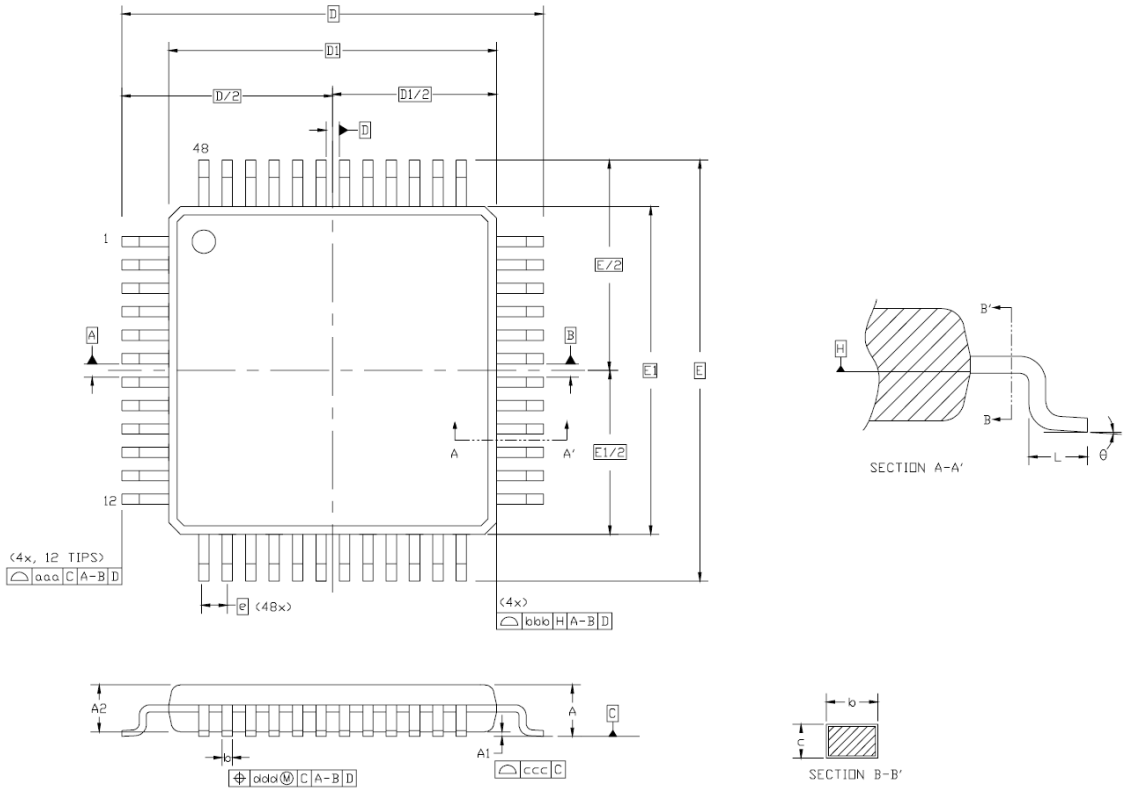
PIN CONFIGURATION

1.1 Pinout



1.2 Package Drawing

TQFP-48 (9x9mm pin outline, 7x7mm housing)



Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	9.00 BSC.		
D1	7.00 BSC.		
e	0.50 BSC.		

Dimension	Min	Nom	Max
E	9.00 BSC.		
E1	7.00 BSC.		
L	0.45	0.60	0.75
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		
θ	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

2 PIN DESCRIPTION

Pin	SIGNAL NAME	Type	Description
POWER & GND & RESET & DEBUG			
10	VDD	S	Supply for the core and IO pads.
11	REGIN	S	Regulator Input. This pin is input to the on-chip voltage regulator
7	GND	S	This is GND signal for power and signal-reference ground for logical signals.
			Decoupling Note: Decouple VDD and GND pin pairs, by placing a ceramic 2.2uF-4.7uF capacitor in parallel with 0.1uf. Route traces from chip pads through the capacitor pads, then to GND/VDD source.
13	RESET#	I/OD	Reset Input and Open Drain output from internal POR. Use 2k pull up to VDD. External reset must be an active low pulse of at least 15uS. See Reset Note
14	DEBUG	I/O	Debug pin for use with upgrade connector
SGPIO INTERFACE SIGNALS			
5/1	SCLK[0/1]	I	SGPIO-SClock Signal for Channel [0/1] See SGPIO Note SCLK0 - SMBUS clock line, If DELL-PROTON protocol is selected
6/2	SLOAD[0/1]	I	SGPIO-SLoad Signal for Channel [0/1] See SGPIO Note SLOAD0 - SMBUS Data line, If DELL-PROTON protocol is selected
4/48	SDO[0/1]	I	SGPIO-SDataOut Signal for Channel [0/1] See SGPIO Note
3/47	SDI[0/1]	OD	SGPIO-SDataIn Signal for Channel [0/1] See SGPIO Note

TYPE: I-Input, O-Output, S-Supply, OD-Open Drain

Pin	SIGNAL NAME	Type	Description
LED INTERFACE SIGNALS			
30,29,28,27, 26,25,24,23	L[0-7]	OD	Connections to LEDs or external latches/flip-flops. Refer to configuration for function
22,21,20,19, 42,41,40,39	L[8-15]	OD	Connections to LEDs, L8 is also used as strapping option during power-up.
SMBUS			
46	I2C_SDA	OD	I2C Data line for Communication with BMC
45	I2C_SCL	OD	I2C Clock line for Communication with BMC
CONFIGURATION AND LATCH ENABLES			
34	CONF0/LEF	I/O	Latch Enable for Fail LEDs (if used) Used as strapping option during power-up
31	CONF1/LEL	I/O	Latch Enable for Locate LEDs (if used) Used as strapping option during power-up
16	CONF2/GA	I/O	Global Activity Pin Used as strapping option during power-up
43	CONF3/LEA	I/O	Latch Enable for Activity LEDs (if used) Used as strapping option during power-up
MATED AND READY LED SIGNALS			
38,37,36,35, 33,32,18,17	M[0-7]	I	Input for detecting drive presence and state of Drive Ready LED signal from SAS/SAS connector
USB SIGNALS			
12	VBUS		VBUS Sense Input. Connect this pin to the VBUS signal of a USB network. Connect VBUS to GND when USB is unused
8	D+	I/O	USB D+
9	D-	I/O	USB D-
PROTOCOL SELECT & Glabal Fail & Activity			
44	SES_SGPIO_SEL /GF	I	Global Fail Indication Pin Used as strapping option during power-up Protocol select input High – SGPIO, Low – SES2
15	NC	I/O	No Connect

TYPE: I-Input, O-Output, S-Supply, OD-Open Drain

2.1 SGPIO Note

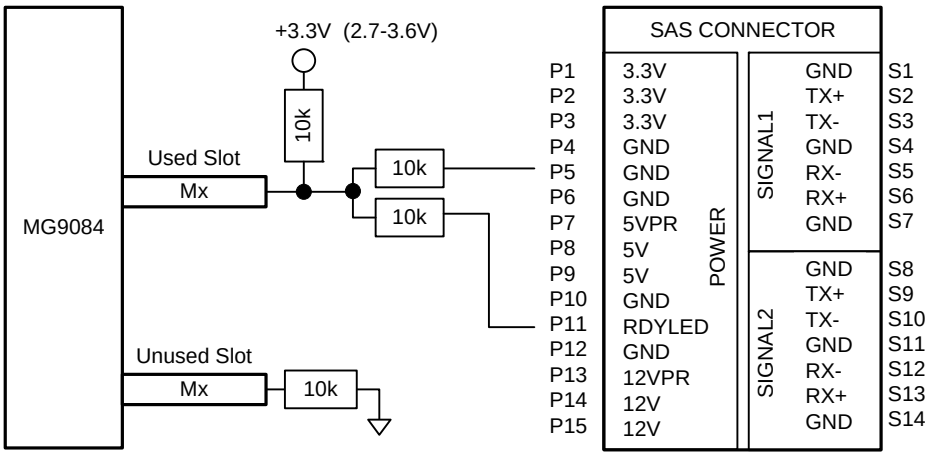
The SDATAIN signals are inputs to the host and outputs from the MG9088. The SDATAOUT signals are outputs from the host and inputs to the MG9088. Connect each SGPIO-pin of the MG9088 to the corresponding pin, matching the signal name. (For example, do NOT connect SDATAIN to SDATAOUT.)

2.2 RESET Note

The RESET-pin is connected to internal Wired-OR logic. The pin should be connected externally to the VDD pin through a 2k pull-up resistor. The MG9088 contains an internal Power-On-Reset circuit, which drives the RESET-pin low until after the VDD has reached a valid level. The MG9088 can be reset by driving the RESET-pin low, however this should be done through an Open Drain buffer. Note that the MG9088 will drive the RESET-pin low when an internal reset-condition occurs.

2.3 Mated and Drive Ready LED signals

The 8 Mx-pins connect to the SAS/SATA connector through a set of resistors. Pin P5 on the SAS/SATA connector is grounded when a drive is installed. If the drive is capable of indicating activity on the Ready LED pin P11 the MG9088 will detect the activity and drive the Activity LED accordingly. Reference circuit for Mx-pin connections:



The reference circuit shows 10k used for all resistors, although other values can be used, as long as they produce the required voltages for each state on the Mx-pins.

See the next section for definitions of the exact voltage levels and interpretations of the Mx pins.

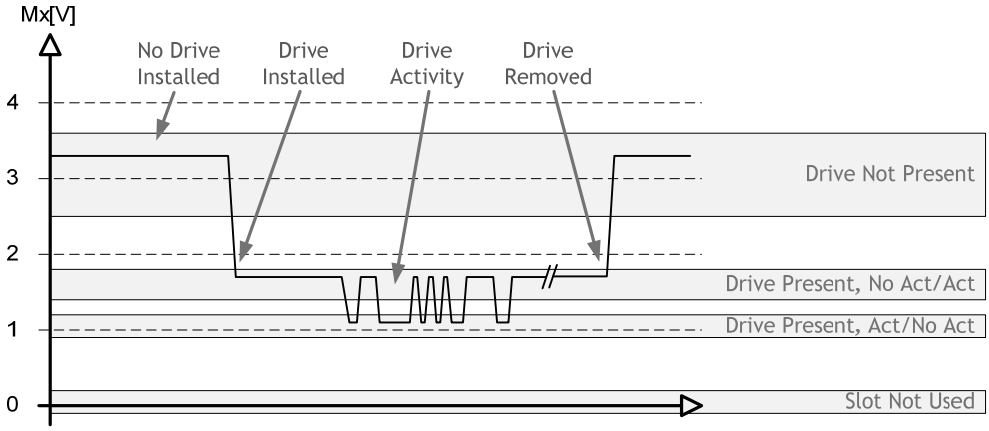
2.4 Mx-pins, States and Pin definitions, SATA vs SAS drives

Some equipment vendors limit the maximum voltage of 2.1V and maximum current draw of 600uA on the Ready LED pin P11. By using 10k resistors as shown in the illustration, a maximum current of 180uA and max voltage of 1.8V is seen on P11.

Most SATA drives have active-low Ready LED pin P11, most SAS drives drive pin P11 low at startup and de-assert the pin during drive activity, but this is not always the case for every model. Some drives regardless of model drive activity exactly as activity happens, and some drives oscillate pin P11 at a set frequency (i.e. 4Hz) during activity.

The MG9088 looks for voltage transition (0 to1 or 1 to 0) on the ready LED pin for activity information, so the default voltage level of the ready LED can either be high or low. Also, the MG9088 will consistently blink the activity LED at 4Hz during the active period to avoid the LED from appearing "off" during periods of extreme activity.

Voltage table and figure below:



If not using 10k (recommended), select resistor values to meet these range targets:

Mx Voltage	Detected State
0.0 - 0.5V	Slot not used
0.5 - 1.3V	Slot used, drive mated with activity (typ SATA) or no activity (typ SAS)
1.3 - 2.7V	Slot used, drive mated without activity (typ SATA) or activity (typ SAS)
2.7 - 3.6V	Slot used, drive not mated

3 ELECTRICAL CHARACTERISTICS

3.1 DC Characteristics

TA=-40°C to 85°C, VDD = 2.7 to 3.6V (Unless Otherwise Noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD			VRST	3.3	3.6	V
I_{SUPPLY}	Supply Current	no IOs driven		26	29	mA
V_{IO}	Voltage on any IO pin or RST# with respect to GND		-0.3		5.8	V
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage			1.0@25mA		V
V_{OH}	Output High Voltage		VDD-0.7			V
I_{IL}	IO-pin Leakage Current	Pin low			1	µA
I_{IH}	IO-pin Leakage Current	Pin high			1	µA
	Supply Current for USB Module(USB Active)	USB Clock = 48MHz		8.69		mA
	Supply Current for USB Module(USB Suspend)	OSC not running		<0.1		mA

3.2 Absolute Maximum Ratings

Operating Temperatures	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on VDD with respect to GND	-0.3V to 4.2V
Maximum total current through VDD to GND	500 mA
Maximum current sunk through any IO-pin	100 mA

Note: Stresses beyond the absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rating for extended period may affect device reliability.

3.3 Reset Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{RST}	RESET# pin threshold Voltage	2.4	2.55	2.7	V
t_{RST}	Minimum Pulse width of reset- pin		15		uS
VDD Ramp Time (1)	VDD = 0V to VDD = V_{RST}V	-	-	1	ms

(1) See Section 5, VDD Ramp time clarification

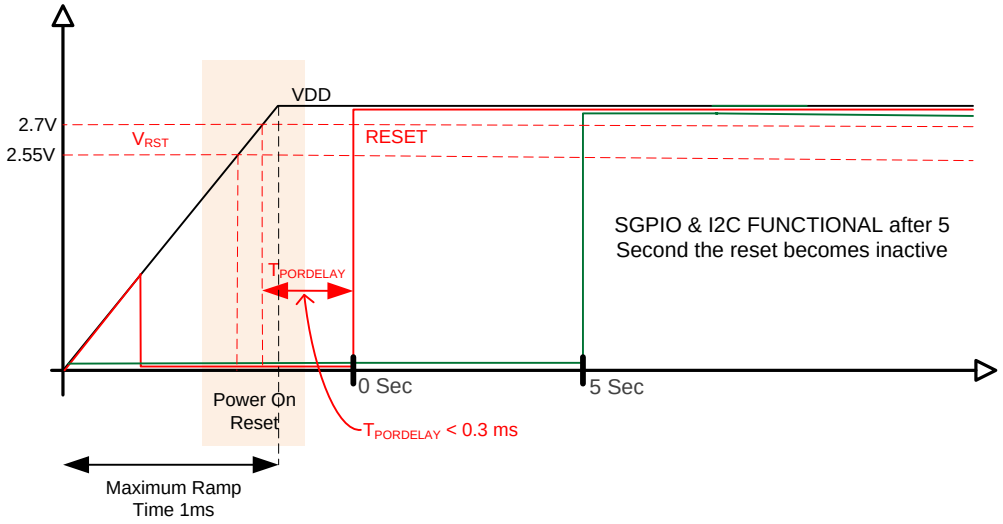
3.4 Voltage regulator Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
REGIN See Note1		2.7		5.25	V
Output Voltage (VDD) See Note2	Output current = 1 to 100mA	3.0	3.3	3.6	V
Output Current				100	mA
VBUS Detection Input Low Voltage				1.0	V
VBUS Detection Input high Voltage		3.0			V
Dropout Voltage See Note3			1		mV/mA

Note1: When external regulator is used, tie to VDD.
Note2: Output Current includes any current required by MG9088
Note3: Minimum Input Voltage is 2.7V or VDD+VDO, whichever is greater

4 SGPIO & SMBUS Readiness

MG9088 takes maximum of 5 second to complete its initialization. During this time the SMBUS requests are not acknowledged and SGPIO host requests are not serviced. System architecture should allow 5 second from the time RESET becomes high before expecting any SMBus commands to be acknowledged by the MG9088. SGPIO and SMBUS modules are functional 5 second after the reset is deasserted.



5 VDD Ramp Time Clarification

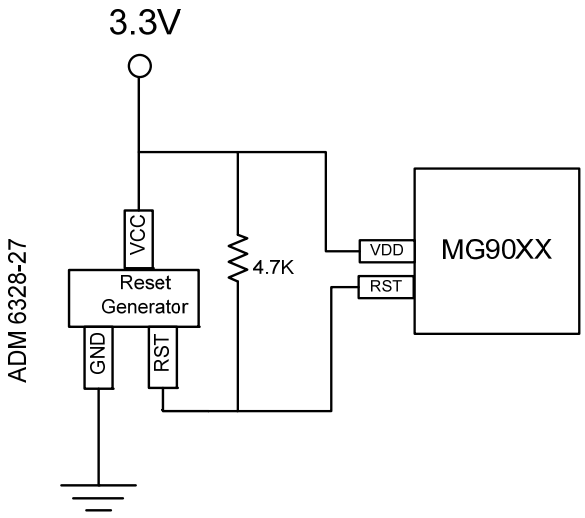
Section 3.3, Reset characteristics specifies the maximum VDD ramp time of 1ms. If the system design can not meet this requirement, a reset generator with open drain output and a minimum reset timeout of 100ms should be added to the MG9088 to avoid unpredictable power up sequence in the device. If the VDD ramp time exceeds 100ms, use reset generator with timeout longer than the VDD stabilization time.

Unpredictable power up will exhibit following behavior:-

1) Device may come out of reset when the VDD have not reached the proper level.

2) Device may not come out of reset in rare instances.

The connection diagram of reset generator is shown below; the reset threshold voltage of 2.7V is selected here.



If more than one device is used in the design, it is recommended to use separate reset generator for every device.

NOTE: Rest generator that monitors a pushbutton/switch closure on the reset output can not be used as it interferes with the in circuit FW upgrade.

6 Latch/No Latch Select

Pin L8 is used as strapping option during power up to determine the latch / no latch configurations.

In no latch mode, the L8 is connected to LEDs which will result in "high" reading during power ON. For the latch mode connect L8 to GND using resistor.

L8	Mode of Operation
High	No Latch
Low	Latch

No Latch Mode:

2 LEDs/slot are driven directly

L0-L7	Directly sinks Activity LEDs 0-7
L8-L15	Directly sinks Status LEDs 0-7
LEA	Not driven
LEF	Not driven
LEL	Not driven

Latch Mode:

3 LEDs/slot are driven using external latches.

L0-L7	Connected to external Latches
L8	Connected to GND.
L9-L15	Not used
LEA	Latch Enable for Activity LEDs
LEF	Latch Enable for Fail LEDs
LEL	Latch Enable for Locate LEDs

7 Device Configuration (strapping options)

At power-up the MG9088 will read a 4-bit.
The configuration is selected according to the following table:

Conf #	Pullup/PullDown				
PIN	43	16	31	34	Description
0	L	L	L	L	
1	L	L	L	H	
2	L	L	H	L	
3	L	L	H	H	
4	L	H	L	L	
5	L	H	L	H	
6	L	H	H	L	
7	L	H	H	H	
8	H	L	L	L	
9	H	L	L	H	
10	H	L	H	L	
11	H	L	H	H	
12	H	H	L	L	
13	H	H	L	H	
14	H	H	H	L	
15	H	H	H	H	

NOTE: See Reference Design section for a list of specific configurations.

L = 3k-10k pull-down resistor from pin to GND
H = 3k-10k pull-down resistor from pin to VDD

It is recommended to include all pull-ups and pull-downs when designing with the MG9088, and use mount options to select the desired configuration.

Configurations for each mode can be specified to support a different number of LEDs, drives, SMBus address, and LED patterns. Thus, the same part-number device can be used in a variety of configurations. Contact AMI for configuration details.

8 LED Blinking Pattern (Dell Proton)

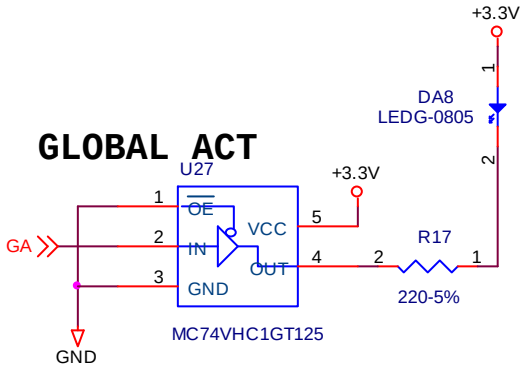
The MG9088 follows the Dell Proton specification blinking pattern and is defined in the following table for various drive states.

SGPIO-SDATAOUT bit:	ODn.0 (Act)	ODn.1 (Locate)	ODn.2 (Fail)	2 LEDS/SLOT		3 LEDS/SLOT		
				Status LED (Green)	Fail LED (Red)	Act LED (Green)	Status LED (Green)	Fail LED (Red)
Description:								
Slot Empty/Drive Not Present	X	X	X	OFF	OFF	OFF	OFF	OFF
Drive Present, No Activity, No side band	0	X	X	ON	OFF	OFF	ON	OFF
Drive Present, No Activity, with side band	0	X	X	X in Proton mode ON in SGPIO mode	X	OFF	X in Proton mode ON in SGPIO mode	X
Drive Present, Activity, No side band	1 or 4Hz	X	X	4Hz	OFF	4Hz	ON	OFF
Drive Present, Activity, with side band	1 or 4Hz	X	X	X	X	4Hz	ON	X
Online	Valid only for SES (Proton) mode			ON	OFF	X	ON	OFF
Locate (Identify)	X	1	0	ON 250 msec OFF 250 msec	OFF	X	ON 250 msec OFF 250 msec	OFF
Fail	X	0	1	OFF	ON 150 msec OFF 150 msec	OFF	OFF	ON 150 msec OFF 150 msec

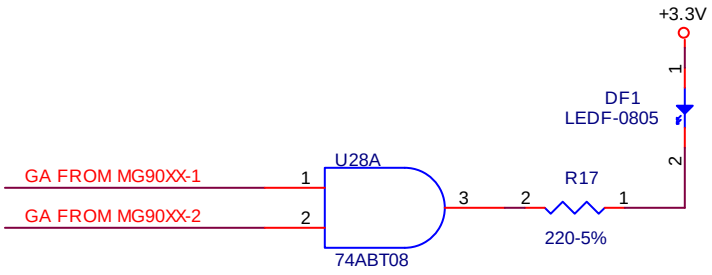
Rebuild	X	1	1	ON 400 msec OFF 100 msec	OFF	X	ON 400 msec OFF 100 msec	OFF
Rebuild	X	X	1Hz	ON 400 msec OFF 100 msec	OFF	X	ON 400 msec OFF 100 msec	OFF
Rebuild Abort	Valid only for SES (Proton) mode			ON 3000 msec OFF 9000 msec	OFF 6000 msec ON 3000 msec OFF 3000 msec	OFF	ON 3000 msec OFF 9000 msec	OFF 6000 msec ON 3000 msec OFF 3000 msec
PFA	X	X	2Hz	ON 500 msec OFF 500 msec OFF 1000 msec	OFF 500 msec ON 500 msec OFF 1000 msec	X	ON 500 msec OFF 500 msec OFF 1000 msec	OFF 500 msec ON 500 msec OFF 1000 msec
Hotspare	X	X	4Hz	ON (if drive present & SGPIO mode)	OFF	X	(if drive present & SGPIO mode)	OFF
In A Critical Array	X	1Hz	X	ON (if drive present & SGPIO mode)	OFF	X	ON (if drive present & SGPIO mode)	OFF
In A Failed Array	X	2Hz	X	ON (if drive present & SGPIO mode)	OFF	X	(if drive present & SGPIO mode)	OFF
(undefined)	X	4Hz	X	ON (if drive present & SGPIO mode)	OFF	X	(if drive present & SGPIO mode)	OFF

9 Global Activity

MG9088 is having support for Global activity on pin16. This signal is active low signal which stays high normally and goes low at the frequency of 4Hz when any one drive has activity. This pin is also used as strapping option during power up, so do not connect the LED directly to this pin. The global activity signal should be connected to a buffer which can be used to drive the global Activity LED. Refer to the reference schematics for more information.

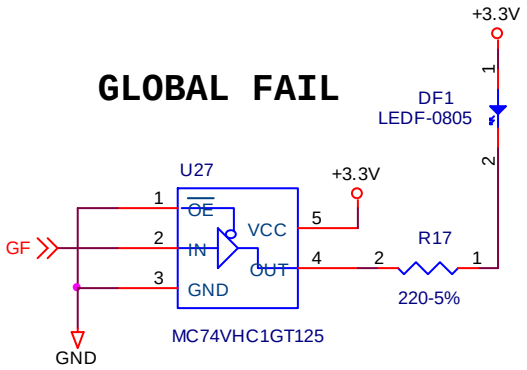


When 2 or more MG9088 is used in the board, the global activity from each chip can be combined using AND gate and then used for driving the global activity LED.

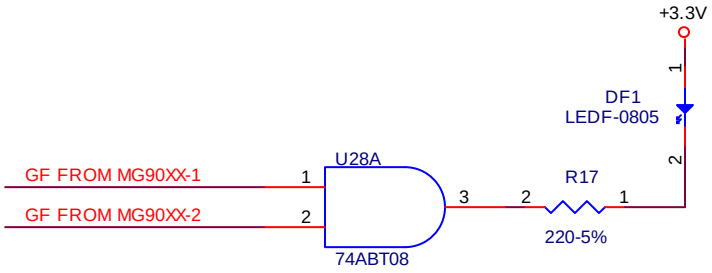


10 Global Fail

MG9088 is having support for Global Fail on pin44. This signal is active low signal which stays high normally and goes low when any one drive fails. This pin is also used as strapping option during power up, so do not connect the LED directly to this pin. The global Fail signal from MG9088 should be connected to a buffer which can be used to drive the global Fail LED. Refer to the reference schematics for more information.



When 2 or more MG9088 is used in the board, the global Fail from each chip can be combined using AND gate and then used for driving the global Fail LED.



11 Configuration Details

There are a total of 16 possible configurations. Some configurations are linked, which means that the same SGPIO interpretation and blinking pattern is used, but SMBus address and SGPIO-offsets are different.

11.1 Configuration 0x00: (linked with conf 0x01, 0x02, 0x03)

Dual Combined SGPIO with up to 8 slot support.

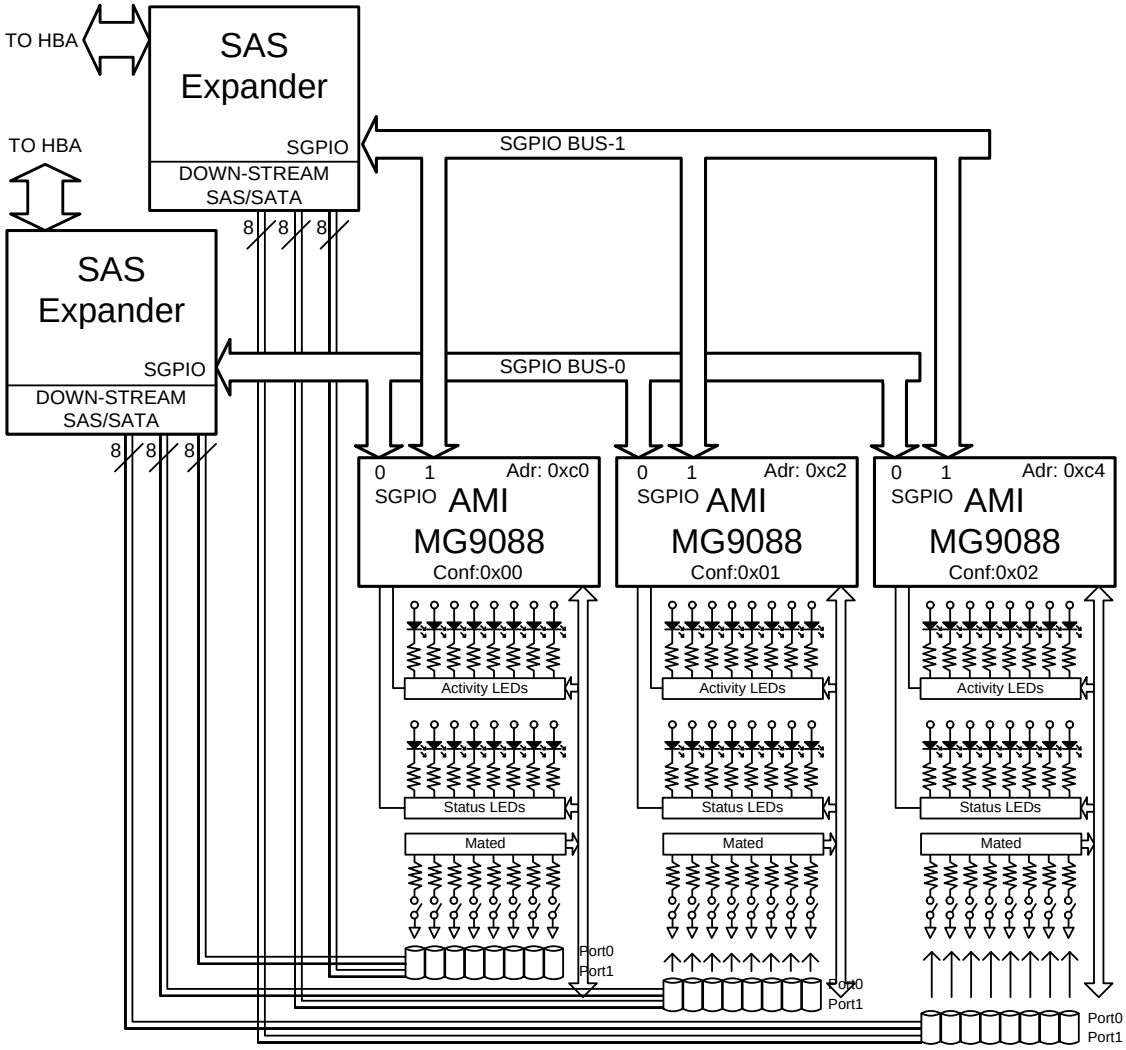
Channels	Dual Channel, all drives on one combined SGPIO channel. Data from two SGPIO initiators is driven to the same set of LEDs
Offset	1of4: First received SGPIO data is driven to first LEDs
SGPIO0	Used, terminate with pull-ups to VDD, even if unused
SGPIO1	Used, terminate with pull-ups to VDD, even if unused
M0-M7	For each used Mx-pin 10k pull-up to 3.3V, 10k series resistor to P5 and 10k series resistor to P11. 10k pull-down to GND for unused slots.
DRL	Drive Ready LED signal from slot is used in combination with activity-bits received on SGPIO to drive the Activity LEDs
I2C	Address 0xc0 – IPMI & SES

SGPIO SDATAIN Bit Assignment:

SDATAIN Bit	Description
IDn.0	Drive Present- Driven to “LOW” to indicate the Drive presence, else stays “HIGH”
IDn.1	Bay Present - Driven to “LOW” to indicate the Bay presence, else stays “HIGH”
IDn.2	Not Used

Blinking Pattern: Refer to section 7

The illustration below shows linked Configurations 0x00, 0x01, 0x02 (the last possible MG9088 for conf 0x03 is not shown here). These sets of configurations are targeted where multiple backplanes are cascaded on the same SGPIO-bus. These configurations also support multi-initiator configurations, which allow two initiators to access the same set of drives through both SAS-ports. The illustration use no latch mode.



11.2 Configuration 0x01: (linked with conf 0x00, 0x02, 0x03)

Dual Combined SGPIO with 8 Activity and 8 Status LEDs directly connected, with offset.

Same as conf 0x00 except:

Offset	2of4: Received SGPIO data is received starting at an offset. The offset depends on how many drives the backplane is configured for.
I2C	Address 0xc2 – IPMI & SES

If the backplane is configured for 8 drives (by no pull-downs to GND on the Mx-bus):
conf 0x01 will drive LEDs starting at SGPIO-drive offset 8.

If the backplane is configured for 6 drives (by pull-downs to GND on the M6-M7):
conf 0x01 will drive LEDs starting at SGPIO-drive offset 6.

If the backplane is configured for 4 drives (by pull-downs to GND on M4-M7):
conf 0x01 will drive LEDs starting at SGPIO-drive offset 4.

If the backplane is configured for 2 drives (by pull-downs to GND on M2-M7):
conf 0x01 will drive LEDs starting at SGPIO-drive offset 2.

11.3 Configuration 0x02: (linked with conf 0x00, 0x01, 0x03)

Dual Combined SGPIO with 8 Activity and 8 Status LEDs directly connected, with offset.

Same as conf 0x00 except:

Offset	3of4: Received SGPIO data is received starting at an offset. The offset depends on how many drives the backplane is configured for.
I2C	Address 0xc4 – IPMI & SES

If the backplane is configured for 8 drives (by no pull-downs to GND on the Mx-bus):
conf 0x02 will drive LEDs starting at SGPIO-drive offset 16.

If the backplane is configured for 6 drives (by pull-downs to GND on the M6-M7):
conf 0x02 will drive LEDs starting at SGPIO-drive offset 12.

If the backplane is configured for 4 drives (by pull-downs to GND on M4-M7):
conf 0x02 will drive LEDs starting at SGPIO-drive offset 8.

If the backplane is configured for 2 drives (by pull-downs to GND on M2-M7):
conf 0x02 will drive LEDs starting at SGPIO-drive offset 4.

11.4 Configuration 0x03: (linked with conf 0x00, 0x01, 0x02)

Dual Combined SGPIO with 8 Activity and 8 Status LEDs directly connected, with offset.

Same as conf 0x00 except:

Offset	4of4: Received SGPIO data is received starting at an offset. The offset depends on how many drives the backplane is configured for.
I2C	Address 0xc6 – IPMI & SES

If the backplane is configured for 8 drives (by no pull-downs to GND on the Mx-bus):
conf 0x03 will drive LEDs starting at SGPIO-drive offset 24.

If the backplane is configured for 6 drives (by pull-downs to GND on the M6-M7):
conf 0x03 will drive LEDs starting at SGPIO-drive offset 18.

If the backplane is configured for 4 drives (by pull-downs to GND on M4-M7):
conf 0x03 will drive LEDs starting at SGPIO-drive offset 12.

If the backplane is configured for 2 drives (by pull-downs to GND on M2-M7):
conf 0x03 will drive LEDs starting at SGPIO-drive offset 6.

11.5 Configuration 0x04:

Dual Combined SGPIO with up to 8 slot support & Group ID support.

Channels	Dual Channel, all drives on one combined SGPIO channel. Data from two SGPIO initiators is driven to the same set of LEDs
Offset	0: First received SGPIO data is driven to first LEDs
SGPIO0	Used, terminate with pull-ups to VDD, even if unused
SGPIO1	Used, terminate with pull-ups to VDD, even if unused
M0-M7	For each used Mx-pin 10k pull-up to 3.3V, 10k series resistor to P5 and 10k series resistor to P11. 10k pull-down to GND for unused slots.
DRL	Drive Ready LED signal from slot is used in combination with activity-bits received on SGPIO to drive the Activity LEDs
I2C	Address 0xc0 – IPMI & SES

Blinking pattern: Refer to Section 7

SGPIO SDATAIN Bit Assignment:

SDATAIN Bit	Description
IDn.0	Drive Present- Driven to "0" to indicate the Drive presence
IDn.1	Bay Present - Driven to "0" to indicate the Bay presence
IDn.2	Group ID

GroupID Bit Assignment:

Group ID Code for Configuration 0x04 is 11b

SDATAIN Bit	Description
ID0.2	Group ID MSB – 1b
ID1.2	Group ID LSB – 1b
ID2.2	Reverse Bay Numbers -1b
ID3.2 to IDn.2	Reserved

NOTE: Please refer to SFF-8485 revision 0.7 for more detail description about the GroupID bits.

11.6 Configuration 0x05:

Same as conf 0x04 except GroupID bit Assignment & I2C address.

I2C	Address 0xc2 – IPMI & SES

Group ID Code for Configuration 0x05 is 10b

SDATAIN Bit	Description
ID0.2	Group ID MSB – 1b
ID1.2	Group ID LSB – 0b
ID2.2	Reverse Bay Numbers -1b
ID3.2 to IDn.2	Reserved

11.7 Configuration 0x06:

Same as conf 0x04 except GroupID bit Assignment & I2C address.

I2C	Address 0xc4 – IPMI & SES

Group ID Code for Configuration 0x06 is 01b

SDATAIN Bit	Description
ID0.2	Group ID MSB – 0b
ID1.2	Group ID LSB – 1b
ID2.2	Reverse Bay Numbers -1b
ID3.2 to IDn.2	Reserved

11.8 Configuration 0x07:

Same as conf 0x04 except GroupID bit Assignment & I2C address:

I2C	Address 0xc6 – IPMI & SES

Group ID Code for Configuration 0x07 is 00b

SDATAIN Bit	Description
ID0.2	Group ID MSB – 0b
ID1.2	Group ID LSB – 0b
ID2.2	Reverse Bay Numbers -1b
ID3.2 to IDn.2	Reserved

11.9 Configuration 0x08:

Dual SGPIO with 8 slot support.

Channels	SGPIO channel-1 drives LEDs for lower 4 drives. SGPIO channel-2 drives LEDs for upper 4 drives. SGPIO channel-1 drives up to 8 slot LEDs when no activity detected on SGPIO Channel-2
Offset	0: First received SGPIO data is driven to first LEDs
SGPIO0	Used, terminate with pull-ups to VDD, even if unused
SGPIO1	Used, terminate with pull-ups to VDD, even if unused
M0-M7	For each used Mx-pin 10k pull-up to 3.3V, 10k series resistor to P5 and 10k series resistor to P11. 10k pull-down to GND for unused slots.
DRL	Drive Ready LED signal from slot is used in combination with activity-bits received on SGPIO to drive the Activity LEDs
I2C	Address 0xc0 – IPMI & SES

Blinking pattern: Refer to Section 7

SGPIO SDATAIN Bit Assignment: Same as configuration 0x04

GroupID Bit Assignment for SGPIO Channel0(111b):

SDATAIN Bit	Description
ID0.2	Group ID Bit1 – 1b
ID1.2	Group ID Bit0 – 1b
ID2.2	Reverse Bay Numbers -1b
ID3.2	Group ID Bit2 – 1b
ID4.2 to IDn.2	Reserved

GroupID Bit Assignment for SGPIO Channel1(110b):

SDATAIN Bit	Description
ID0.2	Group ID Bit1 – 1b
ID1.2	Group ID Bit0 – 0b
ID2.2	Reverse Bay Numbers -1b
ID3.2	Group ID Bit2 – 1b
ID4.2 to IDn.2	Reserved

11.10 Configuration 0x09:

Same as conf 0x08 except I2C Address GroupID bit Assignment:

I2C	Address 0xc2 – IPMI & SES

GroupID Bit Assignment for SGPIO Channel 0(101b):

SDATAIN Bit	Description
ID0.2	Group ID Bit1 – 0b
ID1.2	Group ID Bit0 – 1b
ID2.2	Reverse Bay Numbers -1b
ID3.2	Group ID Bit2 – 1b
ID4.2 to IDn.2	Reserved

GroupID Bit Assignment for SGPIO Channel 1(100b):

SDATAIN Bit	Description
ID0.2	Group ID Bit1 – 0b
ID1.2	Group ID Bit0 – 0b
ID2.2	Reverse Bay Numbers -1b
ID3.2	Group ID Bit2 – 1b
ID4.2 to IDn.2	Reserved

11.11 Configuration 0x0a:

Same as conf 0x08 except I2C Address GroupID bit Assignment:

I2C	Address 0xc4 – IPMI & SES

GroupID Bit Assignment for SGPIO Channel0(011b):

SDATAIN Bit	Description
ID0.2	Group ID Bit1 – 1b
ID1.2	Group ID Bit0 – 1b
ID2.2	Reverse Bay Numbers -1b
ID3.2	Group ID Bit2 – 0b
ID4.2 to IDn.2	Reserved

GroupID Bit Assignment for SGPIO Channel1(010b):

SDATAIN Bit	Description
ID0.2	Group ID Bit1 – 1b
ID1.2	Group ID Bit0 – 0b
ID2.2	Reverse Bay Numbers -1b
ID3.2	Group ID Bit2 – 0b
ID4.2 to IDn.2	Reserved

11.12 Configuration 0x0b:

Same as conf 0x08 except I2C Address GroupID bit Assignment:

I2C	Address 0xc6 – IPMI & SES

GroupID Bit Assignment for SGPIO Channel0(001b):

SDATAIN Bit	Description
ID0.2	Group ID Bit1 – 0b
ID1.2	Group ID Bit0 – 1b
ID2.2	Reverse Bay Numbers -1b
ID3.2	Group ID Bit2 – 0b
ID4.2 to IDn.2	Reserved

GroupID Bit Assignment for SGPIO Channel1(000b):

SDATAIN Bit	Description
ID0.2	Group ID Bit1 – 0b
ID1.2	Group ID Bit0 – 0b
ID2.2	Reverse Bay Numbers -1b
ID3.2	Group ID Bit2 – 0b
ID4.2 to IDn.2	Reserved

11.13 Configuration 0x0c:

Dual SGPIO with 6 Activity and 6 Status LEDs directly connected when activity is detected on both the SGPIO channel

Channels	SGPIO channel-1 drives LEDs for lower 3 drives. SGPIO channel-2 drives LEDs for upper 3 drives. SGPIO channel-1 drives up to 6 slot LEDs when no activity detected on SGPIO Channel-2
Offset	0: First received SGPIO data is driven to first LEDs
SGPIO0	Used, terminate with pull-ups to VDD, even if unused
SGPIO1	Used, terminate with pull-ups to VDD, even if unused
M0-M7	For each used Mx-pin 10k pull-up to 3.3V, 10k series resistor to P5 and 10k series resistor to P11. 10k pull-down to GND for unused slots.
DRL	Drive Ready LED signal from slot is used in combination with activity-bits received on SGPIO to drive the Activity LEDs
I2C	Address 0xc0 - IPMI & SES

Blinking pattern: Refer to Section 7

SGPIO SDATAIN Bit Assignment:

SDATAIN Bit	Description
IDn.0	Drive Present- Driven to “0” to indicate the Drive presence
IDn.1	Bay Present - Driven to “0” to indicate the Bay presence
IDn.2	Group ID

GroupID Bit Assignment for SGPIO Channel0(11b):

SDATAIN Bit	Description
ID0.2	Group ID MSB – 1b
ID1.2	Group ID LSB – 1b
ID2.2	Reverse Bay Numbers -1b
ID3.2 to IDn.2	Reserved

GroupID Bit Assignment for SGPIO Channel1(10b):

SDATAIN Bit	Description
ID0.2	Group ID MSB – 1b
ID1.2	Group ID LSB – 0b
ID2.2	Reverse Bay Numbers -1b
ID3.2 to IDn.2	Reserved

11.14 Configuration 0x0d:

Same as conf 0x0c except I2C Address GroupID bit Assignment:

I2C Address	0xc2 - IPMI & SES

GroupID Bit Assignment for SGPIO Channel 0(01b):

SDATAIN Bit	Description
ID0.2	Group ID MSB – 0b
ID1.2	Group ID LSB – 1b
ID2.2	Reverse Bay Numbers -1b
ID3.2 to IDn.2	Reserved

GroupID Bit Assignment for SGPIO Channel 1(00b):

SDATAIN Bit	Description
ID0.2	Group ID MSB – 0b
ID1.2	Group ID LSB – 0b
ID2.2	Reverse Bay Numbers -1b
ID3.2 to IDn.2	Reserved

11.15 Configuration 0x0e:

Dual SGPIO with 6 Activity, 6 Locate, and 6 Fail LEDs driven directly.

Channels	SGPIO channel-1 drives LEDs for lower 4 drives. SGPIO channel-2 drives LEDs for upper 2 drives.
Offset	0: First received SGPIO data is driven to first LEDs
SGPIO0	Used, terminate with pull-ups to VDD, even if unused
SGPIO1	Used, terminate with pull-ups to VDD, even if unused
M0-M7	For each used Mx-pin 10k pull-up to 3.3V, 10k series resistor to P5 and 10k series resistor to P11. 10k pull-down to GND for unused slots.
DRL	Drive Ready LED signal from slot is used in combination with activity-bits received on SGPIO to drive the Activity LEDs
L0-L5	Directly sinks Activity LEDs 0-5
L8-L13	Directly sinks Fail LEDs 0-5
L6,L7,L14,L15, CONF1, CONF3	Directly sinks Locate LEDs 0-5
LEA	Not driven
LEF	Not driven
LEL	Not driven
I2C	Address 0xc0 – SMBUS & SES

Blinking pattern: Refer to Section 7

SGPIO SDATAIN Bit Assignment:

SDATAIN Bit	Description
IDn.0	Drive Present- Driven to “LOW” to indicate the Drive presence, else stays “HIGH”
IDn.1	Bay Present - Driven to “LOW” to indicate the bay presence, else stays “HIGH”
IDn.2	GroupID

GroupID Bit Assignment for SGPIO Channel0(11b):

SDATAIN Bit	Description
ID0.2	Group ID MSB – 1b
ID1.2	Group ID LSB – 1b
ID2.2	Reverse Bay Numbers -1b
ID3.2 to IDn.2	Reserved

GroupID Bit Assignment for SGPIO Channel1(10b):

SDATAIN Bit	Description
ID0.2	Group ID MSB – 1b
ID1.2	Group ID LSB – 0b
ID2.2	Reverse Bay Numbers -1b
ID3.2 to IDn.2	Reserved

11.16 Configuration 0x0f:

Dual Combined SGPIO with 6 Activity, 6 Locate, and 6 Fail LEDs driven directly.

Channels	Dual Channel, all drives on one combined SGPIO channel. Data from two SGPIO initiators is driven to the same set of LEDs
Offset	0: First received SGPIO data is driven to first LEDs
SGPIO0	Used, terminate with pull-ups to VDD, even if unused
SGPIO1	Used, terminate with pull-ups to VDD, even if unused
M0-M7	For each used Mx-pin 10k pull-up to 3.3V, 10k series resistor to P5 and 10k series resistor to P11. 10k pull-down to GND for unused slots.
DRL	Drive Ready LED signal from slot is used in combination with activity-bits received on SGPIO to drive the Activity LEDs
L0-L5	Directly sinks Activity LEDs 0-5
L8-L13	Directly sinks Fail LEDs 0-5
L6,L7,L14, L15, CONF1, CONF3	Directly sinks Locate LEDs 0-5
LEA	Not driven
LEF	Not driven
LEL	Not driven
I2C	Address 0xc0 – IPMI & SES

Blinking pattern: Refer to Section 7

SGPIO SDATAIN Bit Assignment:

SDATAIN Bit	Description
IDn.0	Drive Present- Driven to “LOW” to indicate the Drive presence, else stays “HIGH”
IDn.1	Bay Present - Driven to “LOW” to indicate the bay presence, else stays “HIGH”
IDn.2	Not Used

NOTE:

1.CONFIGURATIONS 0x00-0x07, & 0x0f: Do not connect the second SGPIO channel for configurations that require only one SGPIO initiator

2. Do not mount the resistor on Ready LED pin, P11 for configurations that do not require the Ready LED logic to control the LEDs,

3. Both the SMBUS (SMBUS & DELL-PROTON) assume the same I2C address

4. Conf 0x0e & 0x0f are not applicable for latch mode

12 Configurations Summary:

List of implemented configurations. All configurations drive the LEDs as "Active Low".

Conf	Number of Drives			I2C address	LEDs	Notes
	SGPIO-0	SGPIO-1	Offset		2 LEDs Direct (no latch): Activity LED & Status LED The Status LED indicates Fail/Locate/Rebuild in a single LED by various blinking pattern in combination with the Activity LED OR 3 LEDs Through latch: Activity LED, Status LED & Locate LED Latch/No Latch selection is done based on L8. L8-High: No latch L8-Low: latch	
0x00	8C	8C	0	0xc0		Combination for support of 32 dual ported drives. LEDs are driven directly. Group ID not supported
0x01	8C	8C	N	0xc2		
0x02	8C	8C	2N	0xc4		
0x03	8C	8C	3N	0xc6		
0x04	8C	8C	0	0xc0		GroupID = 11b
0x05	8C	8C	0	0xc2		GroupID = 10b
0x06	8C	8C	0	0xc4		GroupID = 01b
0x07	8C	8C	0	0xc6		GroupID = 00b
0x08	4/8	4/0	0	0xc0		SGPIO0-GroupID = 111b SGPIO1-GroupID = 110b
0x09	4/8	4/0	0	0xc2		SGPIO0-GroupID = 101b SGPIO1-GroupID = 100b
0x0a	4/8	4/0	0	0xc4		SGPIO0-GroupID = 011b SGPIO1-GroupID = 010b
0x0b	4/8	4/0	0	0xc6		SGPIO0-GroupID = 001b SGPIO1-GroupID = 000b
0x0c	6/3	0/3	0	0xc0		SGPIO0-GroupID = 11b SGPIO1-GroupID = 10b
0x0d	6/3	0/3	0	0xc2		SGPIO0-GroupID = 01b SGPIO1-GroupID = 00b
0x0e	4	2	0	0xc0	3 LEDs Direct (no latch): Activity LED, Status LED & Locate LED	SGPIO0-GroupID = 11b SGPIO1-GroupID = 10b
0x0f	6C	6C	0	0xc0		GroupID = 11b

N=Number of drives in that configuration. C= Combined SGPIO Channel

13 GroupID Explanation

The GroupID is a 2-bit value reported back to the Initiator on the SDataIn-SGPIO-line. This value tells the Initiator which group the set of drives on the backplane belongs to, so that their sequence can be identified correctly in utility software. The GroupID typically groups drives by the number of drives present on each iPass connection to the HBA, which is most typically 4.

For configuration 0x08 to 0x0B, one of the reserved bit is used as group ID, so that maximum of 8 group IDs can be supported to support up to 32 drives. For configuration 0x08 to 0x0B, 4 slots are grouped into one group. Refer to configuration details for more information.

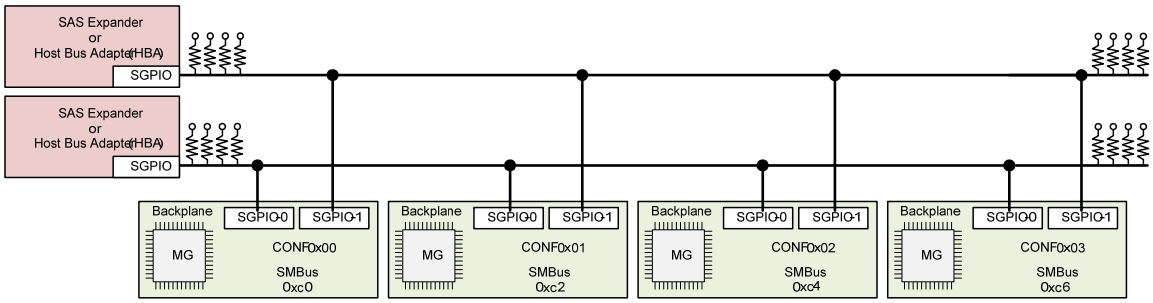
14 Configurations Guide

This section is an architectural overview of each configuration which shows how the various configurations interact with SGPIO-hosts, how configurations are linked, and how the SMBus is routed and accessed across backplanes.

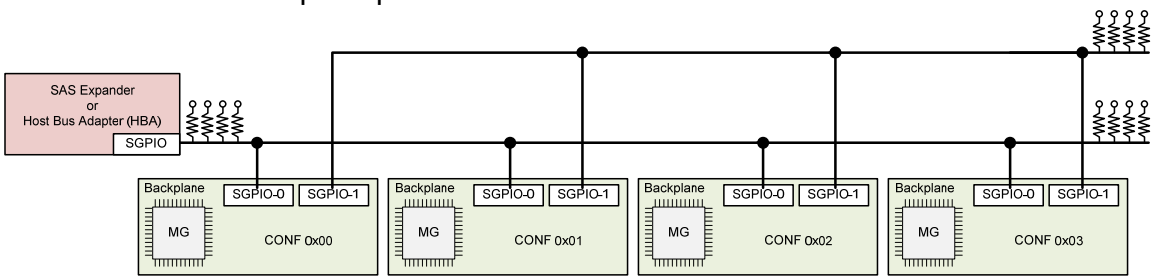
14.1 Configurations 0x00 to 0x03: Dual Initiator with offset-SGPIO.

Up to 2 Initiators (SAS-expander or HBA) per Backplane may be used. Offset-SGPIO means that the SGPIO bus is connected in a "daisy-chain" fashion to each backplane.

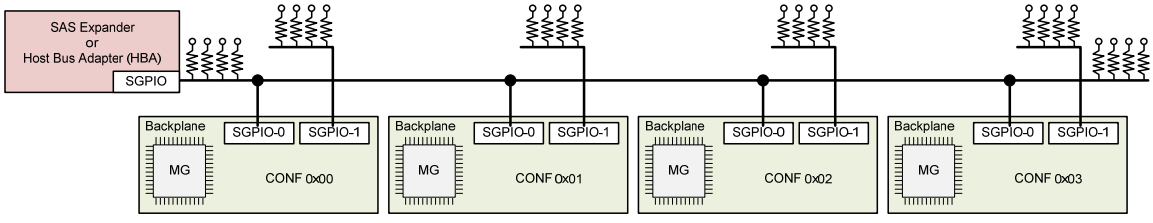
The two SGPIO-data streams are combined by the MG9088. This first illustration shows that of two Initiators connected to 4 backplanes. Note the termination in each physical end of the bus:



A single Initiator can be used as well, in which case the second SGPIO-port should be terminated with weak pull-up resistors as seen below:



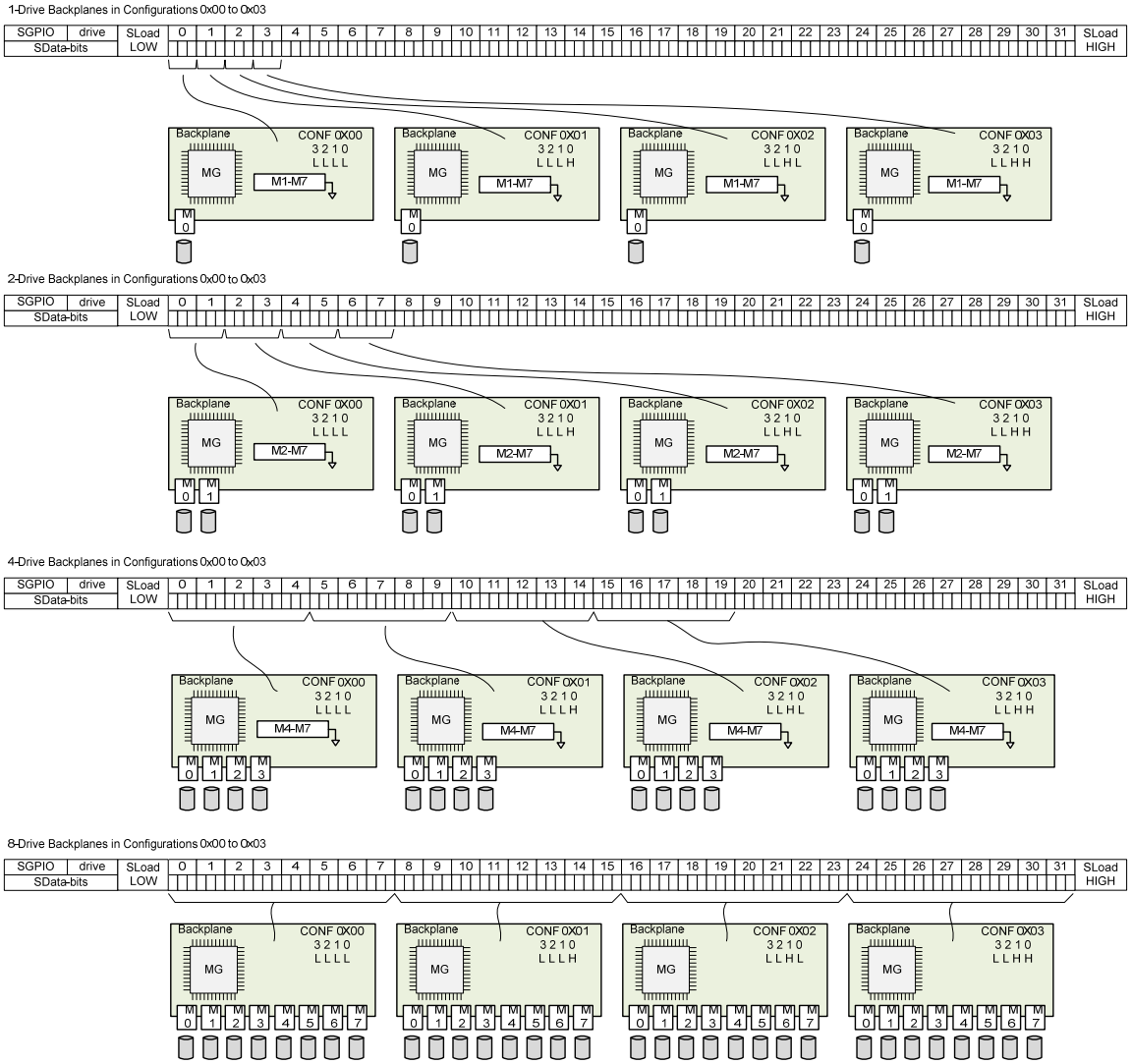
Each unused SGPIO-bus may also be terminated individually on each backplane:



From now on SAS Expanders or HBAs will be categorized as just "INITIATORS".

14.2 Configurations 0x00 to 0x03: SGPIO Offset Mapping

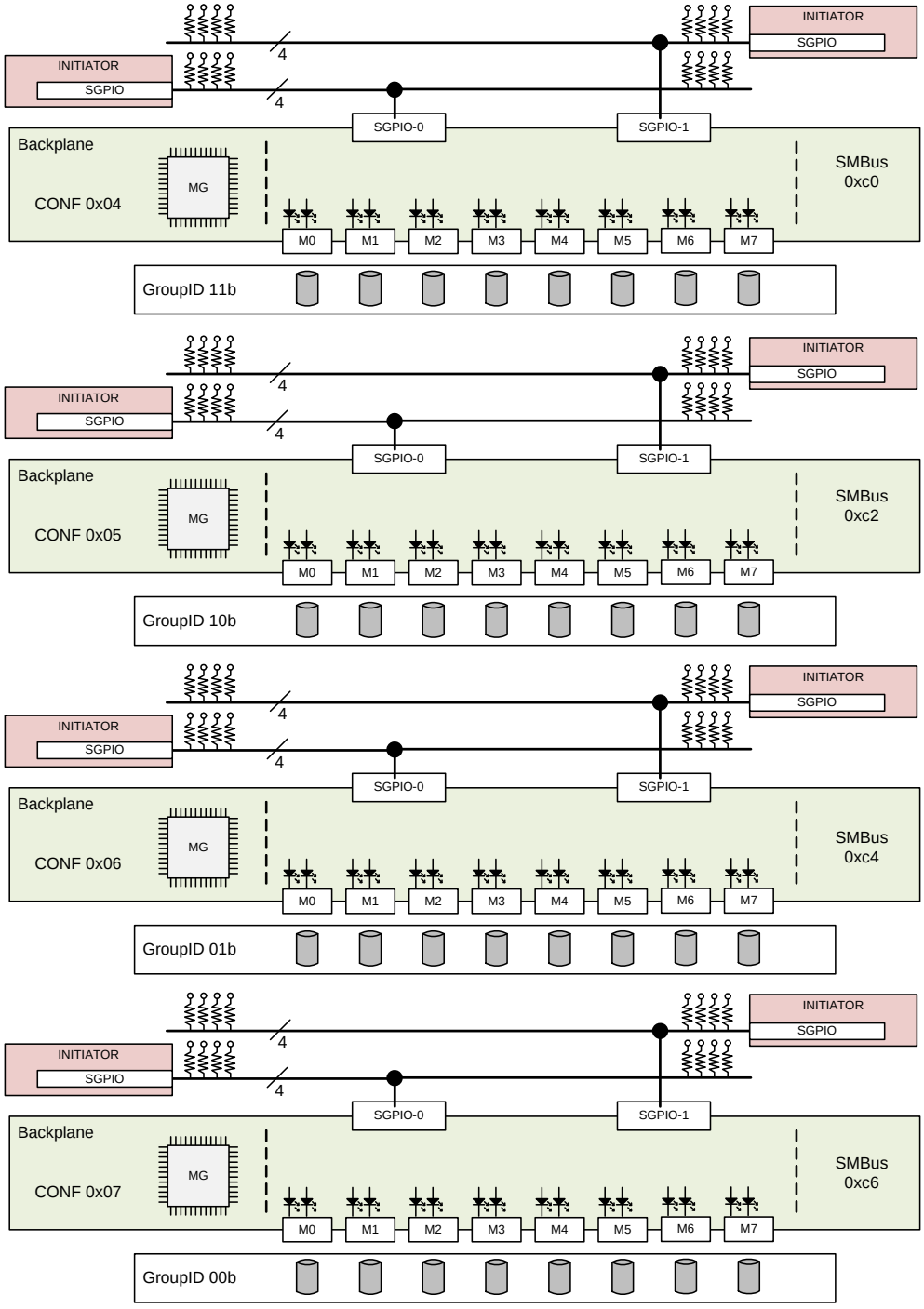
The figure below shows how the drives for each backplane are mapped to the data in the SGPIO-stream, depending on the number of drives on the backplane and the selected configuration:



Note the connections M0 through M7. These are pins on the MG9088 that are grounded for unused drive-slots. The MG9088 scans these pins during power-up to determine how many drives the backplane supports, and uses this number to calculate its offset.

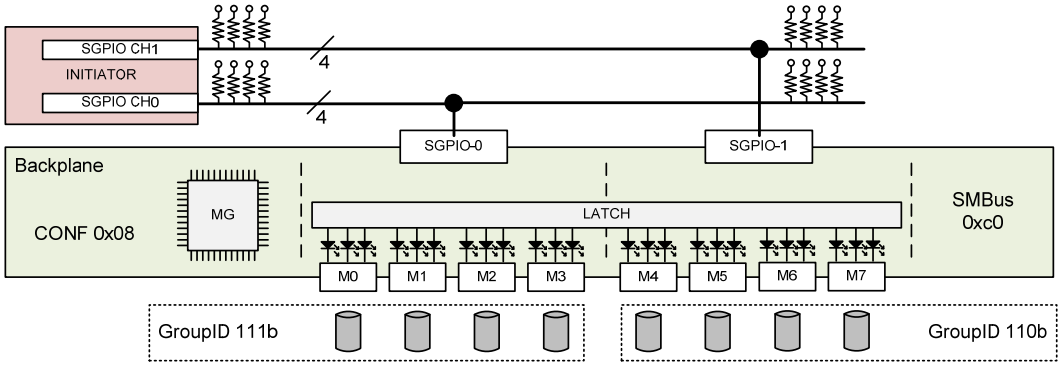
14.3 Configurations 0x04 to 0x07: Dual Initiator with 0-offset SGPIO.

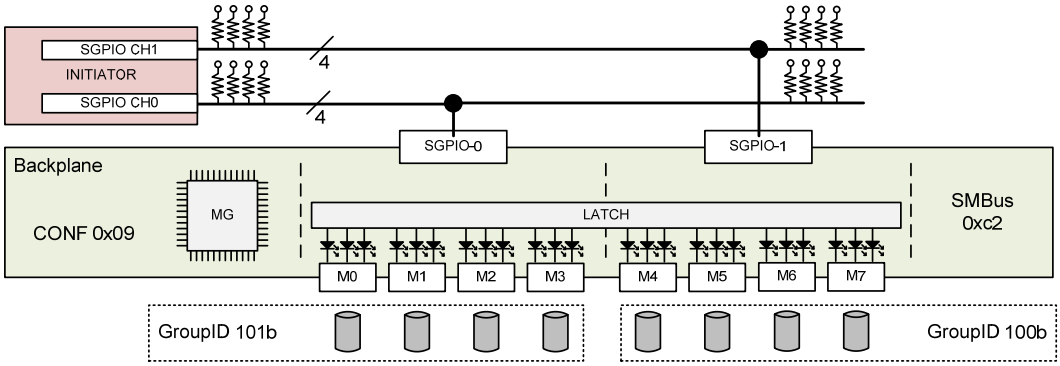
Up to 2 Initiators (SAS-expanders or HBAs) per Backplane may be used, and the SGPIO-offset is 0 for all backplanes. Each backplane has 2 LEDs per slot driven directly. The illustration use the "No latch mode" with 2 LEDs per slot driven directly.

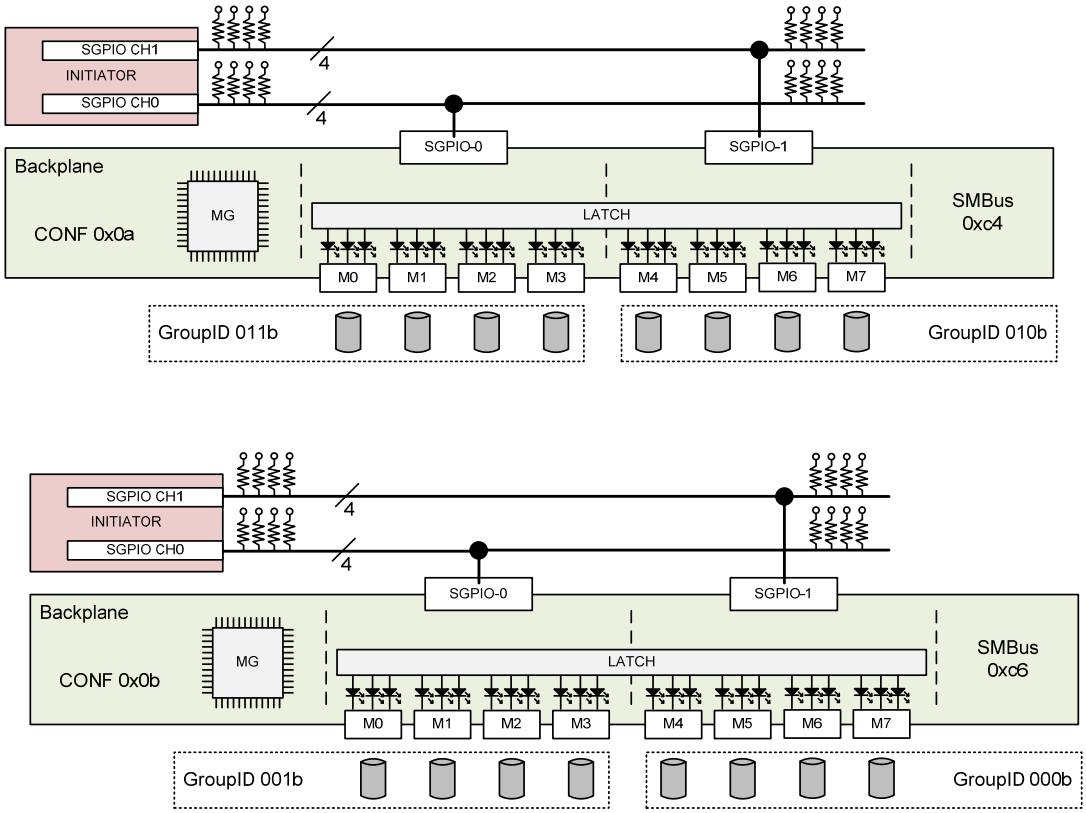


14.4 Configurations 0x08 to 0x0B: Dual SGPIO bus at offset-0 in Latch mode.

These configurations combine the lower 4 drives on SGPIO-0 with the upper 4 drives on SGPIO-1, so that a single MG9088 can be used on two asynchronous SGPIO busses.

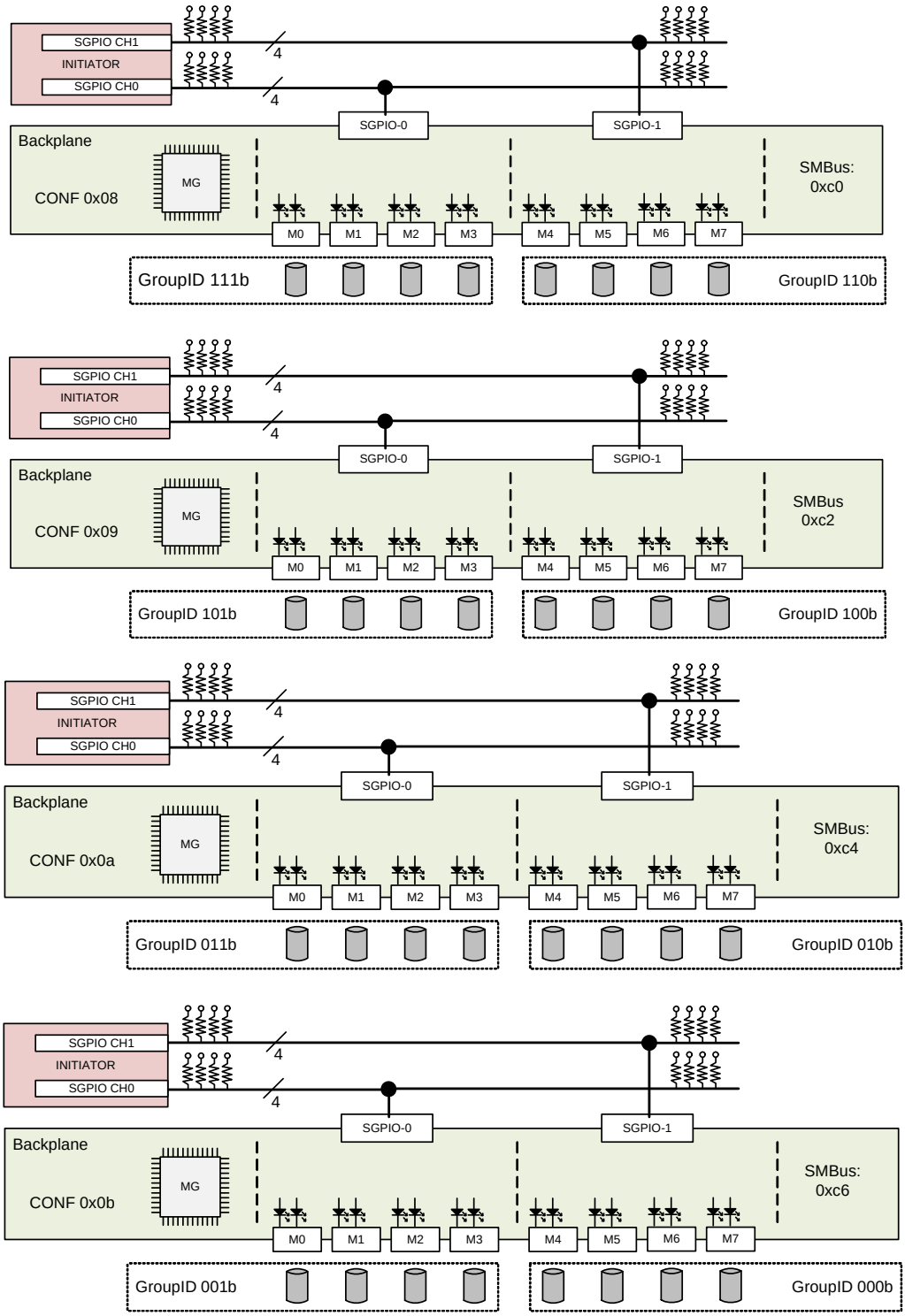






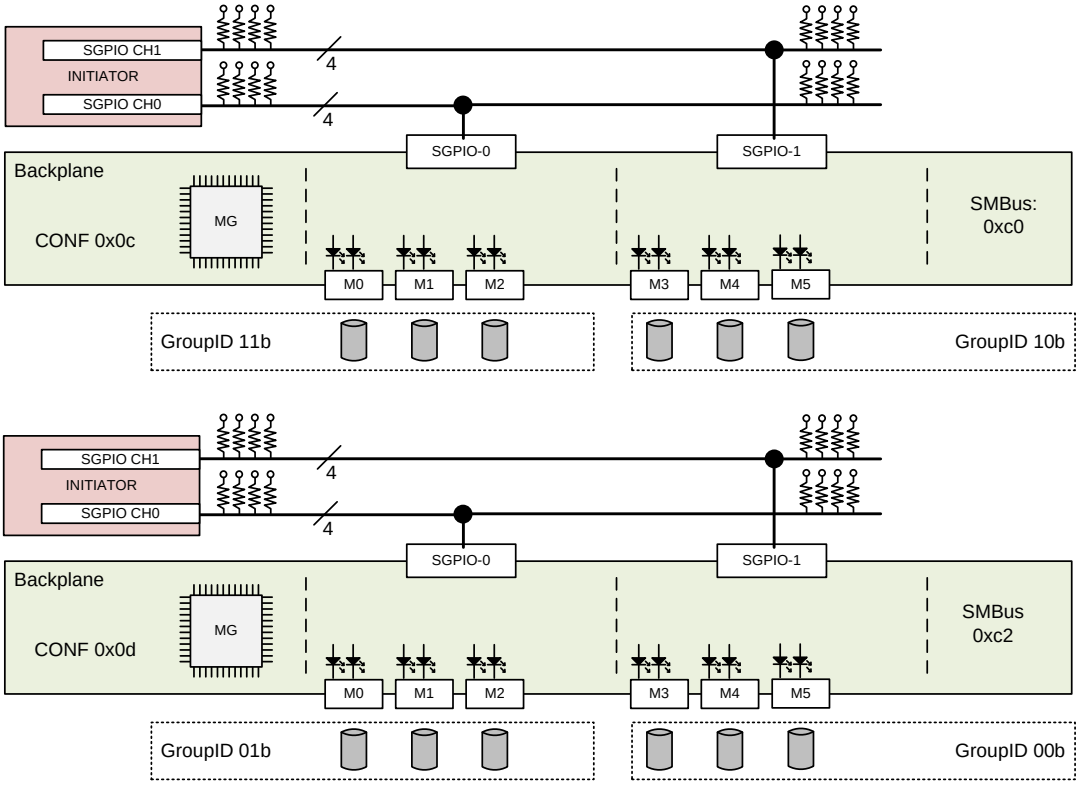
The typical configuration for this is a Host Bus Adapter (HBA) with 2 iPass connections, that each connects to 4 physical drives.

14.5 Configurations 0x08 to 0x0B: Dual SGPIO bus at offset-0 in No Latch mode.



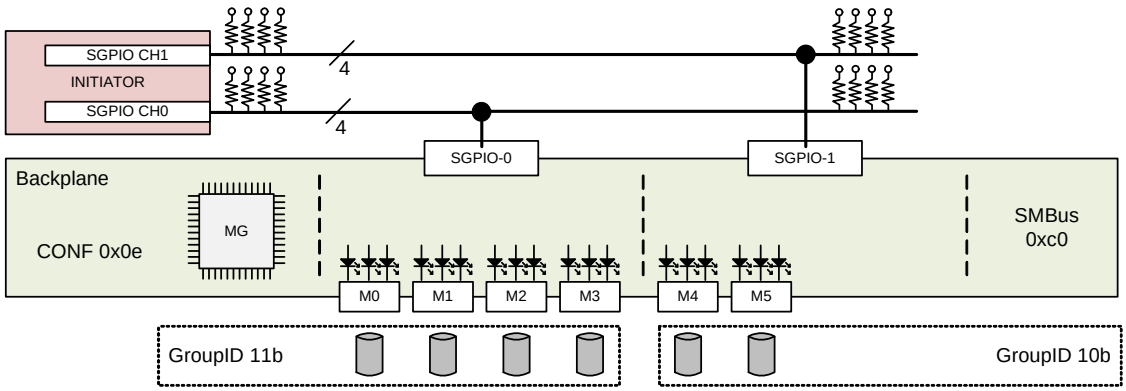
14.6 Configurations 0x0c & 0x0d: Dual SGPIO bus at offset-0

This configuration is architecturally identical to 0x08 and 0x09. The illustration is for no latch mode.



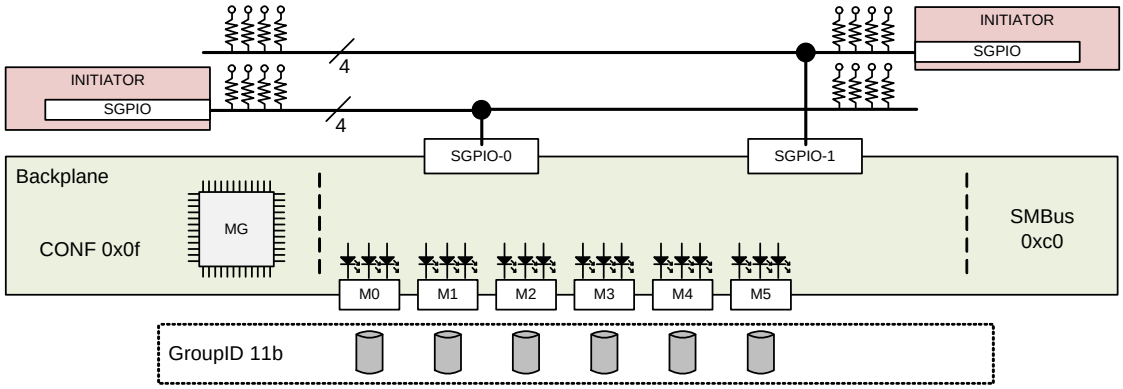
14.7 Configuration 0x0e: Dual SGPIO bus for 6 drives

This configuration is typical with the Intel ESB-2 / ICH-9 type chipsets, where a total of 6 SATA channels are available across two SGPIO ports. For each slot, 3 LEDs are driven directly by the MG9088.



14.8 Configuration 0x0f: Combined Dual Initiator for 6 drives

This configuration targets backplane implementations where two initiators drive the same set of up to 6 drives. Each slot has 3 LEDs driven directly by the MG9088. SGPIO data is combined from the two initiators to drive a single set of LEDs.



15 SGPIO/DELL-PROTON Protocol Select

MG9088 supports the following enclosure management protocols.

1) SCSI Enclosure Services – 2 (DELL-PROTON)
2) SFF-8485 Specification for Serial GPIO (SGPIO)

The SES_SGPIO_SEL pin is read during power on to decide on the protocol.

SES_SGPIO_SEL	Protocol
High	SGPIO
Low	DELL-PROTON

16 SMBUS (IPMI)

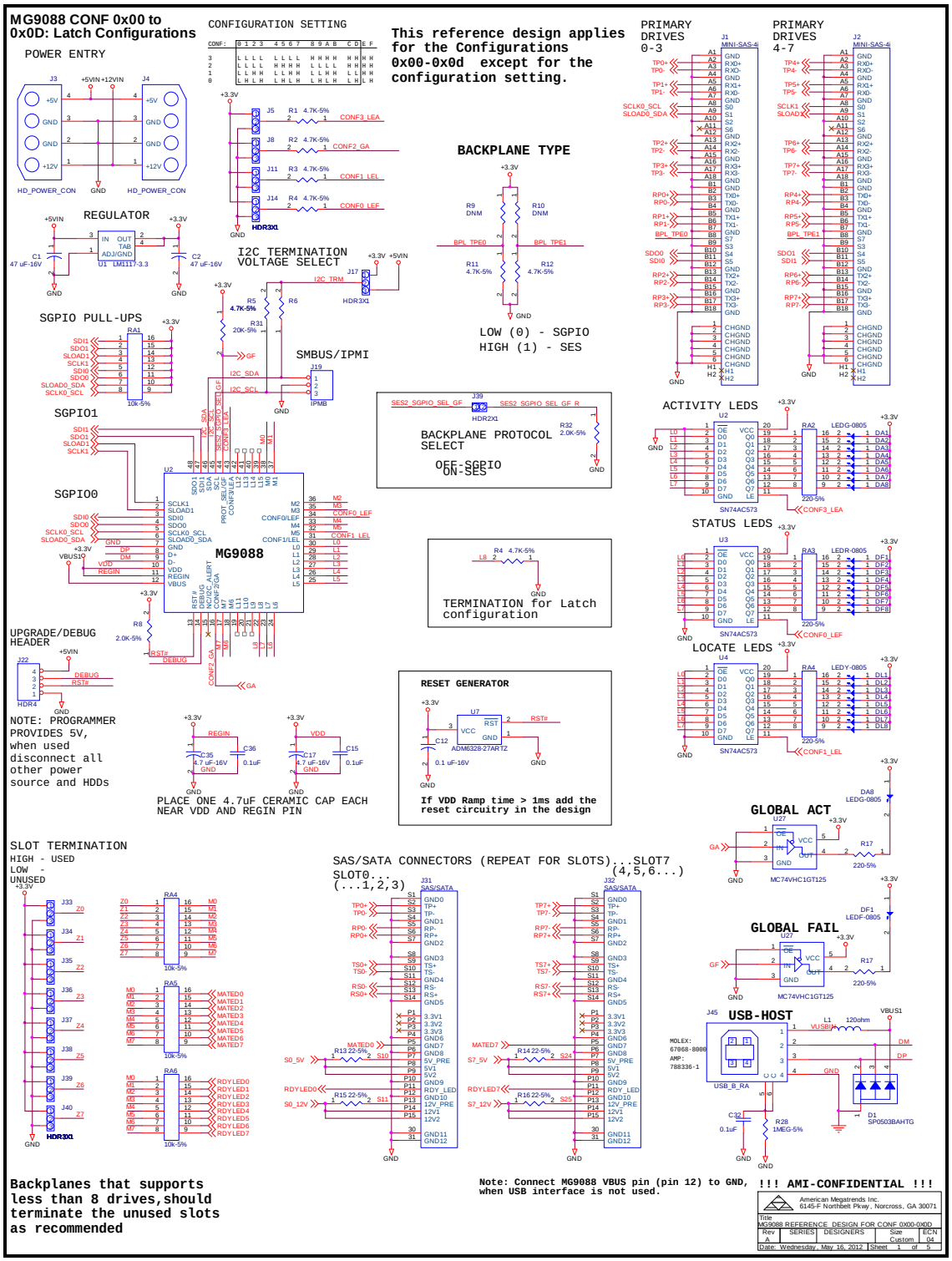
MG9088 has one SMBUS interface to communicate with BMC. The SMBUS supports IPMI-IPMB protocol to interface to BMC. The SMBUS address is determined during power on depending on the configuration. Refet to configuration details for the SMBUS address

17 Reference Designs

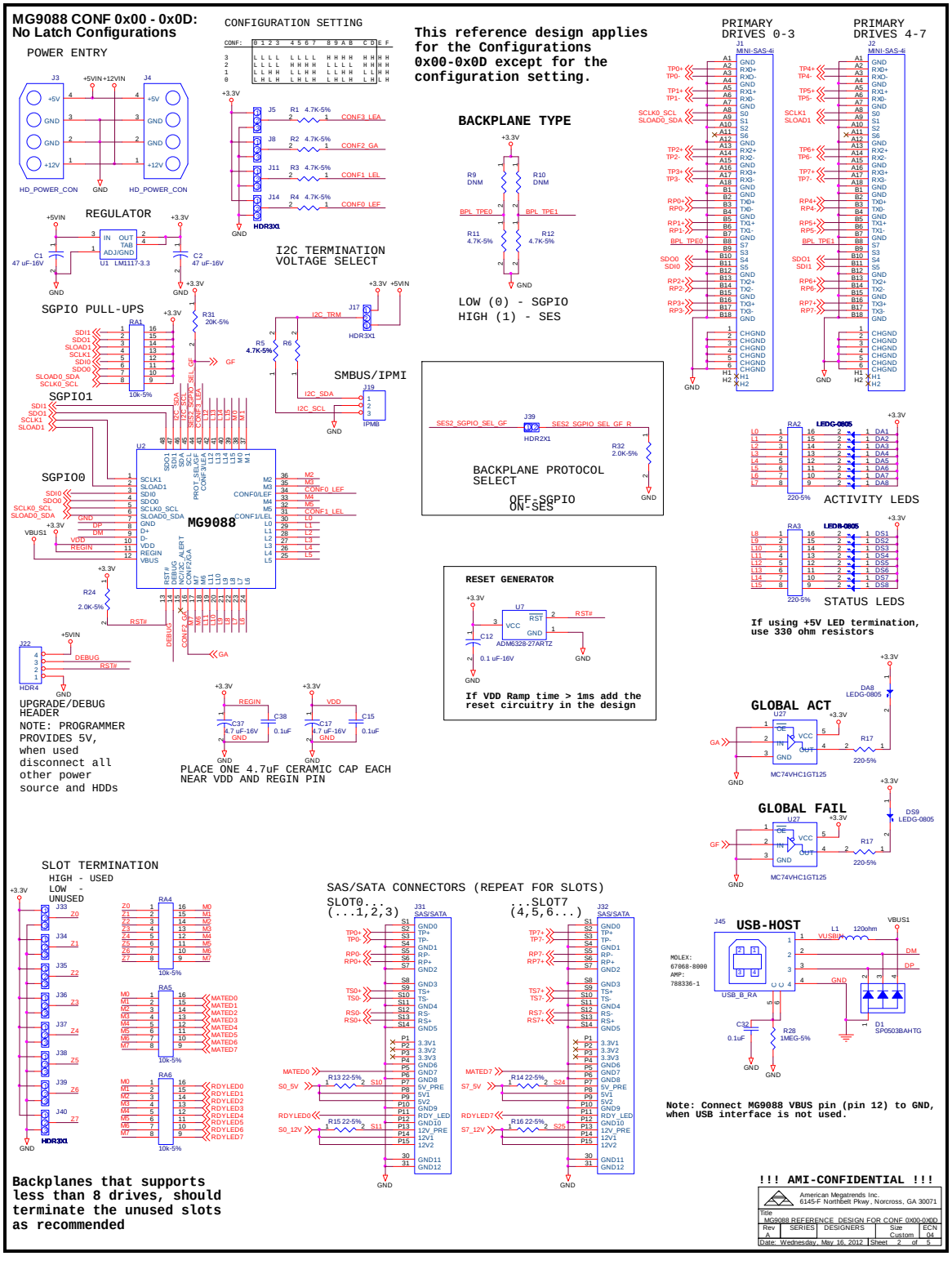
This section shows reference design samples for some sample configurations. Note, schematics and implementations are subject to change. Please contact AMI, and provide your schematic for verification by AMI before finalizing your product.

You can also contact AMI to receive reference design in OrCad Schematic format.

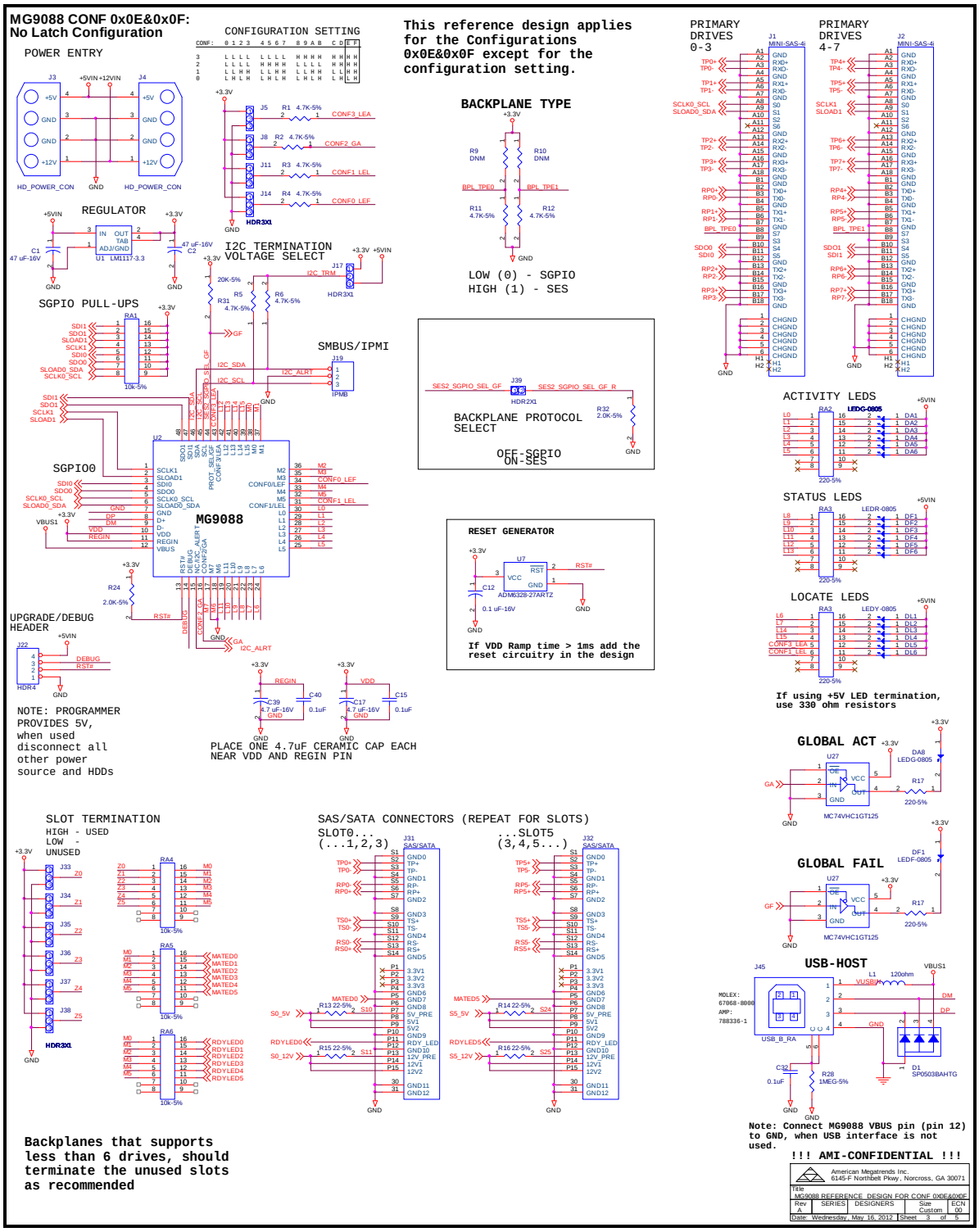
17.1 Latch Configurations 0x0 to 0xD



17.2 No Latch Configurations 0x0 to 0xD



17.3 No Latch Configurations 0xE & 0xF



17.4 Using MG9088 Internal Regulator